



IEC 63601

Edition 1.0 2026-02

# INTERNATIONAL STANDARD

---

**Guideline for evaluating bias temperature instability of silicon carbide metal-oxide-semiconductor devices for power electronic conversion**

## CONTENTS

FOREWORD .....	3
INTRODUCTION .....	5
1 Scope .....	6
2 Normative references .....	6
3 Terms and definitions .....	6
4 Considerations for bias-temperature instability (BTI) stress methods and shift evaluation for SiC-based MOS devices .....	11
4.1 General .....	11
4.2 Mechanisms of $V_T$ shift and hysteresis resulting from PBTI/NBTI stress .....	12
4.3 Threshold voltage and hysteresis measurements .....	12
4.3.1 Comments concerning threshold voltage ( $V_T$ ) measurements .....	12
4.3.2 $V_T$ measurement and conditioning .....	15
4.3.3 Threshold hysteresis ( $V_T^{HYST}$ ) and fast transient effects .....	16
4.4 Typical PBTI/NBTI stress considerations .....	17
4.5 Lifetime prediction models and failure determination .....	18
4.6 Overview of BTI methods .....	20
5 General Measure Stress Measure (MSM) method .....	21
6 Fast Drain Current (FDC) method .....	23
7 Gate sweep MSM method .....	24
8 Conditioning Method .....	26
9 Hysteresis method (or double sense method) .....	27
10 Triple sense method .....	28
Annex A (informative) Supplemental sampling guidelines .....	30
Annex B (informative) Examples demonstrating $V_T$ shift during BTI measurements .....	31
B.1 General .....	31
B.2 Single $V_T$ sense measurements .....	31
B.3 Double $V_T$ sense measurements (hysteresis method) .....	33
B.4 Triple $V_T$ sense measurements ( $V_T$ sense + hysteresis) .....	35
Annex C (informative) Examples demonstrating $V_T$ shift during gate switching .....	37
Annex D (informative) Lifetime models .....	39
Annex E (informative) General introduction to threshold voltage ( $V_T$ ) stability and SiC-based MOS devices .....	41
Bibliography .....	43
Figure 1 – Proposed sweep methods for NBTI and PBTI for MOSFETs .....	14
Figure 2 – Proposed sweep methods for NBTI and PBTI for gated diode configuration .....	14
Figure 3 – Circuit diagram for the $V_T$ measurement using the gated-diode configuration .....	15
Figure 4 – Sweep proposal and $I_D$ vs $V_{GS}$ response for the fixed $V_{GS}$ method .....	15
Figure 5 – Hysteresis measurement sequence, measuring $V_T$ using the gated diode $V_T$ sense method .....	16
Figure 6 – Hysteresis measurement sequence using gate sweeps .....	17

Figure 7 – The absolute value of NBTI $V_T$ shift .....	19
Figure 8 – The PBTI $V_T$ shift as a function of time, fit to a power law for the longer time shift data .....	19
Figure 9 – MSM PBTI stress and measure waveforms .....	22
Figure 10 – MSM NBTI stress and measure waveforms .....	23
Figure 11 – Fast-drain current waveforms for PBTI stress .....	23
Figure 12 – Fast-drain current waveforms for NBTI stress .....	24
Figure 13 – Gate-sweep MSM method waveforms for PBTI .....	25
Figure 14 – Gate-sweep MSM method waveforms for NBTI .....	25
Figure 15 – Conditioning method waveforms for PBTI .....	26
Figure 16 – Conditioning method waveforms for NBTI .....	27
Figure 17 – Conditioning method waveforms for NBTI .....	27
Figure 18 – BTI hysteresis method using the full hysteresis measurement as the $V_T$ sense step after each $V_{GS}$ stress period .....	28
Figure 19 – BTI triple sense method using a first $V_T$ sense followed by a hysteresis measurement (three $V_T$ measurements per sense step) .....	29
Figure B.1 – Example showing the measured $V_T$ over time during PBTI using a single $V_T$ sense .....	32
Figure B.2 – Example showing the measured $V_T$ over time during NBTI using a single $V_T$ sense .....	32
Figure B.3 – Example showing the effect of a conditioning pulse on the measured $V_T$ over time during NBTI using a single $V_T$ sense .....	33
Figure B.4 – Example showing the two $V_T$ versus time curves obtained during the PBTI hysteresis method .....	34
Figure B.5 – Example showing the two $V_T$ versus time curves obtained during the NBTI hysteresis method .....	34
Figure B.6 – Example showing the three $V_T$ versus time curves obtained during the PBTI triple sense method .....	35
Figure B.7 – Example showing the three $V_T$ versus time curves obtained during the NBTI triple sense method .....	36
Figure C.1 – $V_T$ evolution over time .....	38
Table 1 – BTI methods described in this document .....	21

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**Guideline for evaluating bias temperature instability of silicon carbide metal-oxide-semiconductor devices for power electronic conversion****FOREWORD**

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) IEC draws attention to the possibility that the implementation of this document may involve the use of (a) patent(s). IEC takes no position concerning the evidence, validity or applicability of any claimed patent rights in respect thereof. As of the date of publication of this document, IEC had not received notice of (a) patent(s), which may be required to implement this document. However, implementers are cautioned that this may not represent the latest information, which may be obtained from the patent database available at <https://patents.iec>. IEC shall not be held responsible for identifying any or all such patent rights.

IEC 63601 has been prepared by IEC technical committee 47: Semiconductor devices. It is an International Standard.

It is based upon JEDEC JEP184: *Guideline for Evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide Semiconductor Devices for Power Electronic Conversion*. It is used with permission of the copyright holder, JEDEC Solid State Technology Association. It was submitted as a Fast Track document.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2986/FDIS	47/2994/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

This document was developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at [www.iec.ch/members\\_experts/refdocs](http://www.iec.ch/members_experts/refdocs). The main document types developed by IEC are described in greater detail at [www.iec.ch/publications](http://www.iec.ch/publications).

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under [webstore.iec.ch](http://webstore.iec.ch) in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

## INTRODUCTION

The objective of this document is to provide useful definitions and procedures for characterizing the threshold voltage instability of SiC-based power electronic conversion semiconductor (PECS) devices having a gate dielectric region biased to turn devices on and off. This typically refers to MOS (Metal-Oxide-Semiconductor) devices such as field-effect transistors (MOSFETs, Metal-Oxide-Semiconductor Field Effect Transistors)) and insulated-gate bipolar transistors (IGBTs). For simplicity reasons, in the following paragraphs the terms MOSFET or MOS device are used only, while the content is valid for IGBT's as well. Monitoring of threshold-voltage instability in MOS devices is commonly referred to by the term "bias-temperature instability" (BTI), while the applied stress to check for instability is usually referred to as "bias-temperature-stress" (BTS). The terms BTI, BTS, and threshold-voltage instability will be used throughout this document.

## 1 Scope

The scope of this document covers SiC-based PECS devices having a gate dielectric region biased to turn devices on and off. This typically refers to MOS devices such as MOSFETs and IGBTs. In this document, only NMOS (N-type MOS) devices are discussed as these are dominant for power device applications; however, the procedures apply to PMOS (P-type MOS) devices as well.

This document does not define device failure criteria, acceptable use conditions or acceptable lifetime targets. That is up to the device manufacturers and users. However, it provides stress procedures such that the threshold voltage stability over time as affected by gate bias and temperature can be demonstrated and evaluated.

## 2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60747-8:2010, *Semiconductor devices - Discrete devices - Part 8: Field-effect transistors*

IEC 63505, *Guidelines for measuring the threshold voltage ( $V_T$ ) of SiC MOSFETs*

## Bibliography

- [1] IEC 60747-8:2010, *Semiconductor devices - Discrete devices - Part 8: Field-effect transistors*
- [2] J.W. McPherson, *Reliability Physics and Engineering*, Springer New York 2010
- [3] J.H. Stathis, S. Zafar, “*The negative bias temperature instability in MOS devices: A review*”, *Microelectronics Reliability* Vol. 46, 2006, pp. 270–286
- [4] Dieter K. Schroder, “*Negative bias temperature instability: what do we understand?*”, *Microelectronics Reliability* Vol. 47, 2007, pp. 841–852
- [5] James H. Stathis, Souvik Mahapatra, Tibor Grasser, “*Controversial issues in negative bias temperature instability*”, *Microelectronics Reliability* Vol. 81, 2018, pp. 244–251
- [6] JEDEC JEP001A, *Foundry Process Qualification Guidelines*
- [7] JEDEC JEP122H, *Failure Mechanisms and Models for Silicon Semiconductor Devices*
- [8] JEDEC JESD22-A108F, *Temperature, Bias, and Operating Life*
- [9] JEDEC JESD47J.01, *Stress-Test-Driven Qualification of Integrated Circuits*
- [10] JEDEC JESD90, *A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities*
- [11] JEDEC JESD91A, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms*
- [12] JEDEC JESD241, *Procedure for Wafer-level dc Characterization of Bias Temperature Instabilities*
- [13] IEC 63275-1, *Semiconductor devices - Reliability test method for silicon carbide discrete metal-oxide semiconductor field effect transistors - Part 1: Test method for bias temperature instability*
- [14] Thomas Aichinger, Gerald Rescher, Gregor Pobegen, “*Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs*”, *Microelectronics Reliability* Vol. 80, 2018, pp. 68–78
- [15] Daniel B. Habersat, Aivars J. Lelis, Ronald Green, “*Measurement considerations for evaluating BTI effects in SiC MOSFETs*”, *Microelectronics Reliability* Vol. 81, 2018, pp. 121–126
- [16] Katja Puschkarsky, Tibor Grasser, Thomas Aichinger, Wolfgang Gustin and Hans Reisinger, “*Understanding and Modeling Transient Threshold Voltage Instabilities in SiC MOSFETs*”, *International Reliability and Physics Symposium IRPS*, 2018, 3B-5.1-5.10
- [17] Aivars J. Lelis, Ronald Green, and Daniel B. Habersat, “*SiC MOSFET Reliability and Implications for Qualification Testing*”, *International Reliability and Physics Symposium IRPS*, 2017, 2A-4.1-4.4

- [18] Aivars J. Lelis, Daniel Habersat, Ronald Green, Aderinto Ogunniyi, Moshe Gurfinkel, John Suehle, and Neil Goldsman, “*Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements*”, *IEEE Trans. Electron Dev.*, Vol. 55, 2008, pp. 1835-1840
- [19] JEDEC JESD92, *Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics*

---